REMARKS

Section A details the status of the claims. Sections B through G of these Remarks respond to the 35 USC 102 and 103 rejections of the Office Action of June 1, 2004 in the order in which they appeared in the Action.

A. Status of Claims:

Claims 3, 5-9, 12-15, 23-26, 28-29, 32-33 and 36-38, and 40-42 are pending in the application. Claims 20-22, 27, 30-31, 34 and 39 are cancelled in this response. Claims 9, 12-15, 20-21, 24, 26, 27, 30-31, and 34 were rejected under 35 USC 102(e) as being anticipated by Luoh et al., US Publication No. 2003/0017670. Claims 9, 12-15, 21-22, 24, 26-27, 30-31, and 34-40 were rejected under 35 USC 102(e) as being anticipated by Halliyal et al., US Patent No 6,674,138. Claims 3, 5-8, 22-23, 25, 28-29, 32-33, and 41-42 were rejected under 35 USC 103(a) as being unpatentable over Han et al., US Patent No. 5,700,699 in view of Yu et al., US Patent No. 6,184,155. Claims 3, 5-8, 23, 25, 28-29, 32-33, and 41-42 were rejected under 35 USC 103(a) as being unpatentable over Han et al. in view of Luoh et al. Claims 3, 5-8, 23, 25, 28-29, 32-33, and 41-42 were rejected under 35 USC 103(a) as being unpatentable over Luoh et al. in view of Han et al. Claims 9, 12-15, 21, 24, 26-27, 30-31, 34, and 36-40 were rejected under 35 USC 103 as being unpatentable over Halliyal et al. in view of Luoh et al.

B. Claims 9, 12-15, 20-21, 24, 26, 27, 30-31, and 34; 102(e) Rejection

Claims 9, 12-15, 20-21, 24, 26, 27, 30-31 and 34 are rejected under 35 USC 102(e) as being anticipated by Luoh et al.

Claim 9 recites a method for making *a SONOS device*, comprising providing a channel region; providing a first oxide layer on the channel region by an in-situ steam generation process;

providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer, *wherein the device is a SONOS device.*

Referring to FIG. 2 of Luoh et al., which pictures a floating gate memory device, not a SONOS device, the Examiner asserts:

> ... Luoh discloses a method for making a SONOS device, comprising: providing a channel region (area between source and drain 19 [0019]), and providing a first oxide layer 13 on the channel region by ISSG process providing a nitride layer 14, on the first oxide layer 13, and providing a second oxide layer 16 on the nitride layer [0020], wherein the device is a SONOS[sic].

The claim states, in both the preamble and the body, that the device is a *SONOS device.*

In prior responses, Applicants made the following argument: The claim includes the limitation that the device is a SONOS device. The device of Luoh et al. is a floating gate device, not a SONOS device, and thus the claim distinguishes over the device of Luoh et al. This argument still applies. The Examiner responds to this argument in paragraph 11 of the June 1 Action:

> ... it is noted that the feature upon which the Applicant relies, i.e. SONOS layers are being contiguous layers are [sic] not recited in the rejected claim. Although the claim are [sic] interpreted in light of the specification, limitation from the specification are not read into the claim, see *In re Van Geuns* ... Furthermore, it is proper to use the specification to interpret what the applicant meant by a word or phrase recited in the claim. However, it is not proper to read the limitations appearing in the specification into the claim when these limitations are not recited in the claim.

Applicants believe the Examiner to be suggesting that because the term "SONOS device" is used in a claim without being fully defined in the claim, its meaning is uncertain. Applicants refuted this point in the response filed April 23, 2004, by providing ample evidence that the term "SONOS device" is not of Applicants' own devising, nor does it require the description provided in the specification to define it. In this instance the author of the specification has not been his own lexicographer; on the contrary, the term "SONOS device" is a well-known term of art with an established and unambiguous meaning. The Examiner need not look to the present

application for a description of a SONOS device (though such an explanation is provided); examples abound in trade and patent literature, and no limitations need be read into the claim from the specification to provide this meaning. Applicants reiterate this argument.

Claims 12-15 all depend from claim 9, and thus include the limitation that the device is a SONOS device. For the reasons described in this section, the device of Luoh et al. is not a SONOS device.

Claims 20-21 have been cancelled, as has claim 27, from which they depend.

Like claim 9, claims 24 and 26 both include the limitation that the device is a SONOS device, and thus distinguish over the device of Luoh et al.

Claims 30-31 and 34 have been cancelled.

Thus Luoh et al. fail to teach each and every limitation of claims 9, 12-15, 24, and 26, and Applicants respectfully request that the 102(e) rejections of these claims be withdrawn.

C. Claims 9, 12-15, 21-22, 24, 26-27, 30-31, and 34-40; 102(e) Rejection

Claims 9, 12-15, 21-22, 24, 26-27, 30-31, and 34-40 were rejected under 35 USC 102(e) as being anticipated by Halliyal et al., US Patent No. 6,674,138.

Claim 9 recites a method for making a SONOS device, comprising providing a channel region; providing a first oxide layer on the channel region by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer, wherein the device is a SONOS device.

The Examiner points to the channel region 18, oxide layer 28, what he identifies as nitride layer 30, and oxide layer 32 of Fig. 1 of Halliyal et al. The disclosure of Halliyal et al., however, is clear that layer 30 is not a nitride layer. Layer 30 is a "high-K dielectric material" (col. 5, line 10). Halliyal et al. explicitly define the term "high-K dielectric material" to mean "a

dielectric material having a K of about 20 or more" (col. 5, lines 58-59.) As silicon nitride has a K between 6 and 9 (see col. 5, lines 47-48 and Table 1) it is specifically excluded. Claims 12-15 depend from claim 9 and thus also distinguish over Halliyal et al.

Claims 21-22 have been cancelled, as has claim 27, from which they depend.

Claims 24, 26, and 36-38 all include a nitride layer on an oxide layer formed by ISSG and thus distinguish over the device of Halliyal et al. by the same rationale outlined for claim 9.

Claims 30-31, 34, and 39 have been cancelled. Claim 35 was cancelled in a previous response.

Claim 40 formerly recited a method for making a gate dielectric structure for a thin film transistor or a SONOS device, but has been amended to recite only a method for making a gate dielectric structure for a thin film transistor. The device of Halliyal et al. is not taught to be a thin film transistor; thus claim 40 distinguishes over it.

Applicants request that the 35 USC 102(e) rejection of claims 9, 12-15, 24, 26, and 36-38 and 40 be withdrawn.

D. Claims 3, 5-8, 22-23, 25, 28-29, 32-33, and 41-42; 103(a) Rejection

Claims 3, 5-8, 22-23, 25, 28-29, 32-33, and 41-42 were rejected under 35 USC 103(a) as being unpatentable over Han et al. in view of Yu et al.

Claim 3 recites a method for making a transistor containing a gate dielectric structure, comprising providing a gate conductor; providing a channel; and providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process, wherein the transistor is a thin film transistor.

Han et al. shows a thin film transistor having an oxide layer between the gate conductor and the channel, wherein the oxide layer is *not* formed by an ISSG process. The device of Yu et al. is not a thin film transistor. The Examiner states:

> But Yu reference discloses the oxide layer 4b fig. 3 column 3 line 32 by ISSG. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to combine the oxide layer 4b by ISSG of Yu to replace the method of making layer 12 of Han, because it would have created a thin gate oxide layer with reduction in leakage current, during standby, or operating modes as taught by Yu, see abstract.

The Examiner rejects claims 23, 25, and 41-42 using the same rationale.

The device of Han is a TFT device used as the driving circuit in an LCD device (col. 1, lines 19-20.) When standard thermal oxidation is used to form the gate oxide for this TFT device, an expensive substrate must be used which can tolerate the high processing temperatures required by this oxidation (col. 1, line 65 – col. 2, line 1.) One object of the invention is to use a low-temperature method to form the gate oxide (see abstract), allowing a cheaper substrate material to be used (col. 4, lines 6-10.)

The single oxide layer used in most embodiments of Han et al., and the bottom oxide of the ONO stack in the embodiment of Fig. 4 of Han et al., is formed using ECR (Electron Cyclotron Resonance) oxygen plasma (col. 3, lines 10-11, *inter alia.*) The formation of oxide layers by ECR oxygen plasma allows the process to be performed at a relatively low temperature. The temperature can be kept below 600 degrees C (col. 3, lines 63-64.)

The oxide layer of Yu et al., however, is formed using a two-step ISSG process, including a thermal oxidation step performed between 600 and 800 degrees C and an anneal step performed between 800 and 1000 degrees C (col. 3, lines 23-30.) The high temperatures required to form the ISSG oxide layer of Yu et al. would exceed the thermal limitations of the device of Han et al.

Thus Applicants respectfully submit that it would not be obvious to use the ISSG-produced oxide of Yu et al. in the device of Han et al.

The rejections of claims 5-8 similarly rely on the Examiner's suggested combination of Han and Yu; Applicants have explained why the references teach against such a combination. Claim 22 has been cancelled.

Claim 28 depends from claim 3 and thus also distinguishes over the references.

Regarding claims 29, 32 and 33, all three of these claims include the limitation that the thin film transistor comprises a floating gate. The Examiner maintains that "Han discloses a method wherein the transistor is a SONOS transistor ... wherein the transistor comprises a floating gate 7." Han et al., however, nowhere describes layer 7 as a floating gate, referring to it simply as a gate. Layer 7 of the device of Han et al. is a control gate. Charge is applied to a gate (or a control gate) to turn the transistor on, in contrast to a floating gate, which is an electrically isolated or "floating" conductive layer that stores charge. No floating gate appears in any of the embodiments of Han et al., nor is the term used at any point in the reference. No floating gate appear in the device of Yu et al. These claims, then, distinguish over the suggested combination.

In addition, Applicants must emphasize that a SONOS transistor does not and cannot comprise a floating gate. A floating gate device stores charge in a floating gate, which is formed of a conductive material, typically doped polysilicon. A SONOS device stores charge in a dielectric layer, typically a nitride layer. By definition, no floating gate exists in a SONOS device. This point has been made at length in previous responses and will not be repeated here.

Applicants respectfully request that the 35 USC 103 rejection of claims 3, 5-8, 23, 25, 28-29, 32-33, and 41-42 be withdrawn.

E. Claims 3, 5-8, 23, 25, 28-29, 32-33, and 41-42; 103(a) Rejection

Claims 3, 5-8, 23, 25, 28-29, 32-33, and 41-42 were rejected under 35 USC 103(a) as being unpatentable over Han et al. in view of Luoh et al.

Claim 3 recites a method for making a transistor containing a gate dielectric structure, comprising providing a gate conductor; providing a channel; and providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process, wherein the transistor is a thin film transistor.

The Examiner says:

> At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ISSG oxide layer 13 by ISSG process teaching of Luoh to replace the method of making layer 28 Halliyal, because it would have created a high reliability dielectric layer for memory device as taught by Luoh.

Since this rejection is over Han et al. in view of Luoh et al., Applicants assume the Examiner herein names Halliyal in error. The gate oxide 3 of Han et al. is grown by an ECR oxygen plasma process, which, as described in section D of these remarks, is considered advantageous because it can be performed at temperatures below 600 degrees C (col. 3, lines 63-64). Oxide layer 13 of Luoh et al. is produced by an ISSG process in which reaction gases reach a temperature between about 800 and 1200 degrees C.

Section D of these remarks described why it would not be obvious to replace the low-temperature technique of Han et al. with the high-temperature oxidation method of Yu et al. By the same rationale, the use of a low-temperature oxidation technique in Han et al. teaches against use of the high-temperature ISSG method of Luoh et al.

In addition, the oxide layer 13 of Luoh et al. is a blocking oxide between a polysilicon control gate 17 and a polysilicon floating gate 12, the whole in a floating gate memory cell

formed in single crystal silicon. The oxide layer 10 of Han et al. is a gate oxide adjacent to a channel in a non-memory thin film transistor. As these oxide layers serve different roles and exist at different levels in distinct stacks in unrelated devices, Applicants believe that applying the methods used to form one to the formation of the other is in no way obvious.

As the references teach against combination in the manner suggested by the Examiner, Applicants request that the 103(a) rejection of claims 3, 5-8, 23, 25, 28-29, 32-33, and 41-42 be withdrawn.

F. Claims 3, 5-8, 23, 25, 28-29, 32-33, and 41-42; 103(a) Rejection

Claims 3, 5-8, 23, 25, 28-29, 32-33, and 41-42 were rejected under 35 USC 103(a) as being unpatentable over Luoh et al. in view of Han et al.

Claim 3 recites a method for making a transistor containing a gate dielectric structure, comprising providing a gate conductor; providing a channel; and providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process, wherein the transistor is a thin film transistor.

The device of Han et al. is a thin film transistor, while the device of Luoh et al. is not. The Examiner asserts:

> ... Luoh discloses all limitations of claims 3 ... except Luoh does not expressly disclose the device is a thin film transistor. It would have been obvious to one of ordinary skill in the art to use the ISSG teaching of Luoh to form a device for intended use such as thin film transistor for the LCD device, because such device is conventional in the art as it being disclosed by Han ... and would have a high-reliability dielectric layer as taught by Luoh.

The Examiner's suggested motivation for combining steps used to produce selected elements found in the single-crystal floating gate memory cell of Luoh et al. with the non-memory thin film transistor of Han et al. appears to be simply that, at the time of invention, both were known to exist. The Examiner appears to be suggesting that it would have been obvious to

form the device of Luoh et al. as a thin film transistor. There is no suggestion, though, that the memory cell of Luoh et al. would be improved by forming it as a thin film transistor; in fact, it is well known that thin film transistors, because of lower carrier mobilities in the channel region, are slower, have higher leakage, and generally are lower quality transistors than those formed in single crystal silicon.

That the cells are different, with different functions (one a memory cell, the other not), and different structure, and that the oxide layer in each serves an entirely different function has been previously described by Applicants, and applies here as well. The Examiner has provided no motivation to combine the references, and Applicants have described (in section E) why the references themselves teach against such a combination. Thus claim 3 distinguishes over the applied references. The remaining claims distinguish for the same reason.

Claim 28 additionally includes the limitation that the device is a SONOS device. The device of Luoh et al., as described in detail in this and prior responses, is a floating gate device, not a SONOS device. No suggestion has been identified (or is apparent) to modify the floating gate device of Luoh to transform it to a SONOS device; thus this claim further distinguishes over the references both together and separately.

Applicants thus request that the 103(a) rejection of claims 3, 5-8, 23, 25, 28-29, 32-33, and 41-42 be withdrawn.

G. Claims 9, 12-15, 21, 24, 26-27, 30-31, 34, and 36-40; 102(e) Rejection

At paragraph 9 of the Office Action of June 1, 2004, the Examiner says that claims 9, 12-15, 21, 24, 26-27, 30-31, 34, and 36-40 were rejected under 35 USC 102(e) as being anticipated by Halliyal et al. in view of Luoh et al.

As more than one reference was applied, Applicants assume the rejection under 35 USC 102(e) was made in error. Applicants assume this rejection was intended to be made under 35 USC 103, and will respond to it as such.

Claim 9 recites a method for making a SONOS device, comprising providing a channel region; providing a first oxide layer on the channel region by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer, wherein the device is a SONOS device.

The Examiner suggests it would have been obvious to use the ISSG method of Luoh et al. to form oxide layer 28 of Halliyal et al. "because it would have created a high reliability dielectric layer for memory device as taught by Luoh."

The oxide layer 28 of Halliyal et al. is a gate oxide in a SONOS device, while the oxide layer 13 of Luoh et al. is part of a blocking dielectric between control gate 17 and floating gate 12 in a floating gate device. As noted in the response to prior rejections, the unrelated structure and function of these devices, and the unrelated function of the oxide layer in each, provides no motivation to pick and choose processing steps used in each and combine them to produce the elements of the claim with improper hindsight reconstruction as the only apparent guide.

Claims 12-15, 24, 26, 36-38 and 40 distinguish for the same reason. Claims 21, 30-31, 34, and 39 have been cancelled.

In addition, claim 40 has been amended to recite a method for making a gate dielectric structure for a thin film transistor, comprising providing a gate conductor; providing a channel region; and providing, between the gate conductor and the channel region and in contact with the channel region, an oxide layer of a gate dielectric structure by an in-situ steam generation process performed at a temperature ranging from about 600 to about 1050 degrees Celsius, a pressure

ranging from about 100 millitorr to about 760 torr, and for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms, *wherein the gate dielectric structure is for a thin film transistor.* As neither the device of Halliyal et al. nor the device of Luoh et al. teaches a thin film transistor, the claim clearly distinguishes over any combination of them.

As there is no motivation to combine the references in the manner suggested, Applicants respectfully request that this rejection of claims 9, 12-15, 24, 26, 36-38, and 40 be withdrawn.

CONCLUSION

In view of these amendments and remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. **If any objections or rejections remain, Applicants respectfully request an interview to discuss the references.** If the Examiner has any questions, he is asked to contact the undersigned agent at (408) 869-2921.

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